40Gbps QSFP+ Transceiver (UQSFP-LR4)

CWDM4 10km LC

Features

- Compliant with 40G Ethernet IEEE802.3ba and 40GBASE-LR4 Standard
- QSFP+ MSA compliant
- Compliant with QDR/DDR Infiniband data rates
- Up to 11.2Gb/s data rate per wavelength
- 4 CWDM lanes MUX/DEMUX design
- Up to 10km transmission via SMF
- Operating case temperature: 0 to 70℃
- Maximum power consumption 3.5W
- Dual LC receptacle
- RoHS compliant

Applications

- InfiniBand QDR, DDR and SDR
- 40G Ethernet
- Proprietary High Speed Interconnections
- Data center

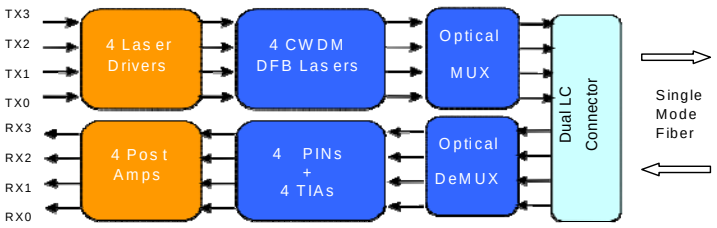
Part numbers

P/N	*Data Rate*	*Wavelength*	*Connector*	*Distance*
UQSFP-LR4	40Gbps	1310Tx SM	Dual LC	10km

Description

UQSFP-LR4 module converts 4 inputs channels of 10Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

Transceiver Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	TST	-40	85	℃	
Relative Humidity(non-condensing)	RH	0	85	%	
Operating Case Temperature	TOPC	0	70	℃	
Supply Voltage	VCC	-0.3	3.6	V	
Input Voltage	Vin	-0.3	Vcc+0.3	V	

Recommended Operating Environment

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	TOPC	0		70	degC
Power Supply Voltage	VCC	3.13	3.3	3.47	V
Power Consumption		-		3.5	W
Data Rate	DR		10.3		Gbps
Link Distance with G.652	D	2		10	km

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter						
Side Mode Suppression Ratio	SMRS	30			nm	
Average Launch Power, each lane	PAVG	-7		+2.3	dBm	
Total Average Launch Power	P-T			+8.3		
Optical Modulation Amplitude (OMA)	POMA	-4.0		+3.5	dBm	1
Difference in Launch Power between any two lanes	Ptx,diff			6.5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane	OMA-TDP	-4.8	-		dBm	1
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	Rin			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	RT			-12	dB	
Transmitter Eye Mask Margin	EMM	10			%	2
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	

Receiver						
Damage Threshold	THd	+3.3			dBm	
Overload, each lane	OVL	+2.3			dBm	
Receiver Sensitivity in OMA, each Lane	SEN			-12.6	dBm	
Difference in Receive Power between any two Lanes (OMA)	Prx,diff			7.5	dB	
Signal Loss Assert Threshold	LOSA	-28			dBm	
Signal Loss Deassert Threshold	LOSD			-15	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receive Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			12.3	GHz	

Notes:

1. Transmitter wavelength, RMS spectral width and power need to meet the OMA minus TDP specs to guarantee link performance.
2. The eye diagram is tested with 1000 waveform.

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Power Consumption				3.5	W
Supply Current	Icc			1.1	A
Differential Input	Zin	90	100	110	Ohm
Differential Input Voltage Swing Threshold		50		1100	mVp-p
Differential output voltage Swing		300		850	mVp-p
Differential Output	Zout	90	100	110	Ohm
Bit Error Rate	BR			E-12	

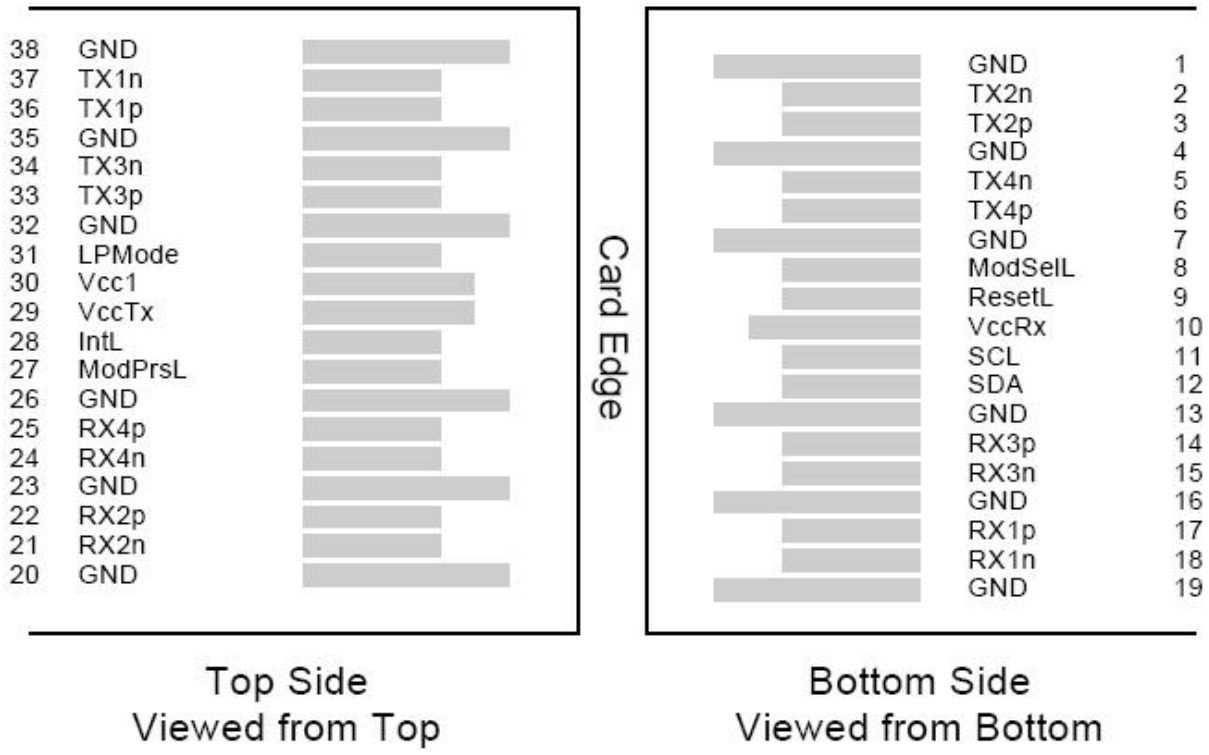
Pin Descriptions

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1

33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module. GND is the symbol for signal and supply (power) common for QSFP modules.
2. The connector pins are each rated for a maximum current of 500mA.



ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module

settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

PSM LR4operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

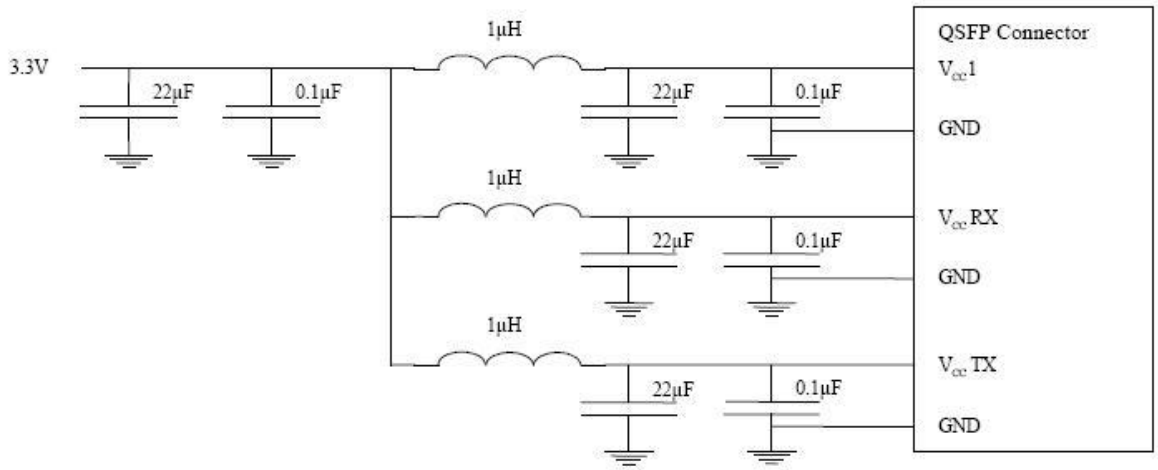
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure1.

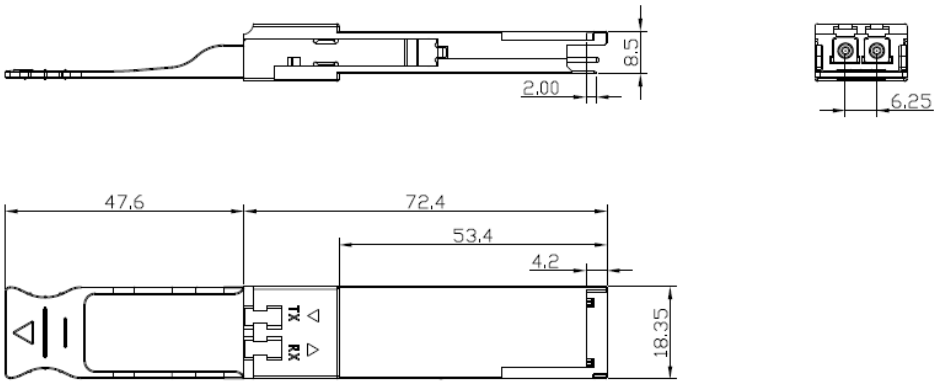


Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all QSFP+ LR4. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in Figure 3. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

Parameter	Symbol	Min	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	+3	degC	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-2	2	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%	10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-2	2	dB	Per channel

Mechanical Dimensions



ESD

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007)

For More Information

USource Technology
F8 Huameiju, Yulv RD
Shenzhen China 518102
Tel. +68-755-23014563
info@usourcetech.com
www.usourcetech.com